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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,055	06/24/2003	Gianluca Blasi	32079-00087USPX	8552

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EXAMINER	
JACOB, MARY C	

ART UNIT	PAPER NUMBER
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,055	BLASI ET AL.	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b)

Status

1)☒ Responsive to communication(s) filed on *21 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other. _____.

DETAILED ACTION

1. The response filed on 12/21/06 has been received and considered. Claims 1-28 are presented for examination.

Drawings

2. Previous objections to the drawings not repeated below have been withdrawn in view of the amendments to the specification, filed 12/21/06.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 559. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. The objection to claim 6 is withdrawn in view of the amendments to the claims filed 12/21/06.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 6-8, 10, 15, 16, 19, 21, 22, 23, 26, 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al ("A Goal Tree Based High-Level Test Planning System for DSP Real Number Models", Proceedings of the International Test Conference, pages 1000-1009, October 18-23, 1998).

7. As to Claims 1, 8, Lin et al teaches: a computer based test bench generator for verifying integrated circuits specified by models in a Hardware Description Language, comprising: a repository storing a general set of self-checking tests applicable to integrated circuits (section 2, lines 14-16; section 4.1, paragraph 5); means for entering behavior data of an integrated circuit model (section 3, paragraph 2, lines 2-5); means for entering configuration data of the integrated circuit model (section 6); means for automatically generating test benches in said Hardware Description Language, said means being configured to make a selection and setup of suitable tests from said repository according to the specified integrated circuit model, configuration and behavior data (section 2, lines 22-29; section 3, paragraph 1, lines 1-3; section 6).

8. As to Claims 15 and 22, Lin et al teaches: a test bench generator for integrated circuit designs, comprising: a repository which stores functional and structural characteristic data for integrated circuit models (Figure 1, VHDL Primitive Library, Specification Repository); a processing functionality which receives an identification of a specific integrated circuit model to be tested along with model data describing the configuration and behavior of that specific integrated circuit model, the processing functionality operating to: process the model data in view of the identified specific integrated circuit model to produce a configured integrated circuit model suitable for simulation; and compare the specific integrated circuit model to characteristic data in the repository to identify tests applicable to that specific integrated circuit model (section 2, lines 10-29; section 3, paragraphs 1 and 2; section 4.1, paragraph 5; Figure 6 and description).

9. As to Claims 3 and 10, Lin et al teaches: wherein said general set of tests is specified in said Hardware Description Language (section 3, paragraph 1, lines 1-3).

10. As to Claim 6, Lin et al teaches: wherein said configuration data is input to said generator through a command line (Figures 4-6).

11. As to Claim 7, Lin et al teaches: wherein said selection of tests is based on conditional statements (page 1004, first 2 lines, item 3; Figure 7).

12. As to Claims 16 and 23, Lin et al teaches: wherein the processing functionality further processes the identified tests which are applicable to produce a set of self-checking test benches for the specific integrated circuit model (section 2, lines 26-27; Figure 1, "VHDL Simulator").

13. As to Claims 19 and 26, Lin et al teaches: wherein the integrated circuit models in the repository, as well as the received specific integrated circuit model to be tested, are specified using a hardware description language (section 2, lines 11-15, lines 22-25; section 3, paragraph 2, lines 2-5).

14. As to Claim 21, Lin et al teaches: further including a simulator functionality which applies the identified applicable tests against the configured integrated circuit model (section 2, lines 26-27; Figure 1, "VHDL Simulator").

15. As to Claim 28, Lin et al teaches: further including applying the identified applicable tests against the configured integrated circuit model to simulate operation (section 2, lines 26-27; Figure 1, "VHDL Simulator").

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

18. Claims 2, 4, 5, 9, 11-14, 17, 20, 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al as applied to claims 1. 8. 15 and 22 above, in view of Bollano et al ("The Virtual Intellectual Property Library: From Paradigm to Product", Proc. Of IP99 Conference, Santa Clara, March 1999).

19. As to Claims 2, 4, 5, 9, 11-14, 17, 20, 24 and 27, Lin et al teaches a test bench generator for verifying integrated circuits wherein the hardware description language is VHDL (section 2, lines section 3, paragraph 1, lines 1-3; section 3, paragraph 2, lines 2-5); wherein said configuration data is input to said generator through a command line (Figures 4-6); wherein said configuration data is input to said generator through a command line (Figures 4-6).

20. Lin et al does not expressly teach: wherein the integrated circuit model is a memory model, wherein the hardware description language can be Verilog, or wherein said behavior data is specified in proprietary language.

21. Bollano et al teaches a system that implements a soft IP library in the design flow to shorten the design time and lower the design cost by making system know-how available as customizable, reliable and reusable design blocks through the use of a Virtual Intellectual Properties library that is composed of system level modules written in VHDL (page 1, column 1), wherein said integrated circuit model is a memory model (page 3, column 2, lines 5-8); wherein said hardware description language can be VHDL or Verilog (page 4, column 2, last paragraph, first sentence); wherein said

behavior data is specified in proprietary language (pages 4-5, "IP Code Protection") and wherein the user can set up scenario and parameter values through a menu for use of the modules and functional verification and validation is carried out through RTL simulation using the VIP test bench modules for pattern generation and response analysis (page 3, column 2, "Simulation, verification and characterization").

22. Lin et al and Bollano et al are analogous art because they are both directed to the testing and validation of integrated circuits defined in a hardware description language using test benches.

23. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the integrated circuit model as defined by Lin et al with a memory model, Verilog code or proprietary language as taught by Bollano et al since Bollano et al teaches a system that implements a soft IP library in the design flow to shorten the design time and lower the design cost by making system know-how available as customizable, reliable and reusable design blocks through the use of a Virtual Intellectual Properties library that is composed of system level modules written in VHDL (page 1, column 1).

24. Claims 18 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al as applied to Claims 15 and 22 above, in further view of Killian et al (U.S. Patent 6,477,683).

25. As to Claims 8 and 25, Lin et al teaches a test bench generator for integrated circuit designs wherein the processing functionality further processes the identified tests

which are applicable to produce a set of self-checking test benches for the specific integrated circuit model (section 2, lines 26-27; Figure 1, "VHDL Simulator").

26. Lin does not expressly teach wherein the self-checking test benches include self-checking models incorporating complex constructs for comparing data, waiting for internal events, and timing constraint checking with respect to the specific integrated circuit model.

27. Killian et al teaches a method that automatically configures a processor by generating both a description of a hardware implementation of the processor in HDL and a set of development tools such as a compiler, assembler, debugger and simulator for programming the processor from the same configuration specification (column 6, lines 32-60), which allows for a complete flow for configuration of processor hardware and software including feedback from hardware design results and software performance to aid selection of optimal configuration for the design instead of hardware and software configuration alone (column 8, lines 54-61). The method taught by Killian et al includes a test bench for integrated circuit designs that incorporates complex constructs for comparing data (column 33, lines 25-27), waiting for internal events (column 33, lines 56-59; column 34, lines 61-62), and timing constraint checking with respect to the specific integrated circuit model (column 23, lines 14-17, lines 34-40, lines 48-50).

28. Lin et al and Killian et al are analogous art because they are both directed to the design and verification of integrated circuit designs described in HDL using a test bench.

29. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the test benches as taught in Lin et al to include constructs for comparing data, waiting for internal events and checking timing constraints as taught by Killian et al since Killian et al teaches a method that allows for a complete flow for configuration of processor hardware and software including feedback from hardware design results and software performance to aid selection of optimal configuration for the design instead of hardware and software configuration alone (column 8, lines 54-61).

Response to Arguments

30. Applicant's arguments filed 12/21/07 have been fully considered but they are not persuasive.

31. Applicant argues that the recited sections of Lin do not mention a general set of self-checking tests applicable to integrated circuits or the storage of such tests in a repository (page 14).

32. The recited sections of Lin teach test plans that define "groups of tests" that guide the testing process (section 2, lines 14-16). Each "test group" defines a series of organized test cases and maps to a partially specified configuration declaration of the test bench (section 4.1, paragraph 5). The Test Bench Generator contains these "partially specified configuration declarations" and each test scenario or "test group" maps to one of the configuration declarations of the test bench to then develop specific test benches for each test scenario (section 3, paragraph 2, lines 11-14). It was

concluded that these "partially specified configuration declarations" define a "general set of self-checking tests applicable to integrated circuits" that are stored in a repository as disclosed by the discussion of library based test bench development wherein the VHDL primitives can be reused for test bench development as discussed (section 3, paragraph 3). It is further noted that Lin teaches a file I/O strategy that promotes the reuse of test files by varying test file names and allowing a test group to sequence through a list of enumerated test files (section 4.4, last paragraph and section 7, paragraph 2 last sentence and section 7, paragraph 4, last sentence) which further shows that tests are stored in a repository for further use.

33. Applicant argues that the Lin system will not "automatically generate test benches in said Hardware Description Language" based on "a selection and setup of suitable tests from said repository".

34. The recited sections of Lin teach that the Test Bench Generator takes specific requirements, the model under test and stimulus generator from the VHDL primitive library to create a test bench for the simulation system (section 2, lines 22-25). It is further recited that the whole testing process is automated (section 2, lines 27-29). Lin also teaches that the Test Bench Generator is commanded to create and execute a set of test benches to answer a specific query (section 6). It is understood that the Test Bench Generator contains partially specified "configuration declarations" and each test group maps to one of these partially specified configuration declarations wherein a specific test bench is then created (section 3, paragraph 2, lines 11-14; section 4.1, paragraph 5). In light of these teachings in Lin, it is concluded that test benches are

"automatically generated in said Hardware Description Language" wherein the partially specified configuration declaration is chosen from a repository based on the mapping of the test group to this configuration declaration or the "query" that is defined by the user, and then the Test Bench Generator creates and executes the set of test benches for the specified test group or to answer the specific query. The "configuration declaration" is specified and "selected" from a repository based on the "mapping" or "query", and the suitable tests are "set up" by creating and executing a set of test benches specific to the test cases or query.

35. Applicant argues the tests in Lin are not identified based on a processing comparison of the model to the circuit characteristic data as claimed (page 15).

36. The recited sections of Lin teach comparing the specific integrated circuit model to characteristic data in the repository to identify tests applicable to that specific integrated circuit model. Lin teaches a Test Bench Generator that contains partially configured "configuration declarations" of the test bench wherein the test bench is a VHDL model (section 3, paragraph 1, lines 1-3, paragraph 2, lines 11-14). These "configuration declarations" contain functional and structural characteristic data as disclosed in the recited sections. Because Lin teaches library-based test bench development wherein the use of "configuration declarations" allows test benches to be reconfigured (section 1, paragraph 3), it was determined that these "configuration declarations" are stored in a repository for re-use. Lin teaches that when it is necessary to identify tests applicable to a test group, the test group maps to one of these partially specified configuration declaration in the test bench (section 4.1, paragraph 5),

therefore, determining which configuration declaration in the repository is needed for the specific test and further uses the configuration declaration containing the characteristic data to generate a specific test bench for the specified test case (section 3, paragraphs 2 and 3). It was concluded that the "mapping" of the test groups would define a "specific" test bench, or integrated circuit model, needed to identify tests for the specific case, and therefore the applicable partially specified "configuration declarations" are searched for and found in the Test Bench Generator wherein the configuration declarations contain characteristic data. These teachings were determined to encompass the processing and comparison steps recited in the claim language.

Conclusion

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

38. Buckley, Jr. (US Patent 6,490,711) teaches a test bench creation tool that is to be integrated into typical EDA design tool suites, that provides a designer with an ability to classify parts of a design using such techniques as special comment lines. Once the parts of a design have been classified in this manner, the tool (or alternatively, the designer) selects pre-existing test bench HDL design templates suitable for the identified circuit classes.

39. Allard (US Patent 7,024,346) teaches a method for generating a test bench including the steps of: providing an integrated circuit (IC) having a cell containing an analog component and including an ATAP, providing an AATG having at least one

default cell; loading a cross-reference file; selecting tests required for cells in the cross-reference file by default; and generating a test bench.

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Mary C. Jacob
Examiner
AU2123

MCJ
2/16/07

2/16/07

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